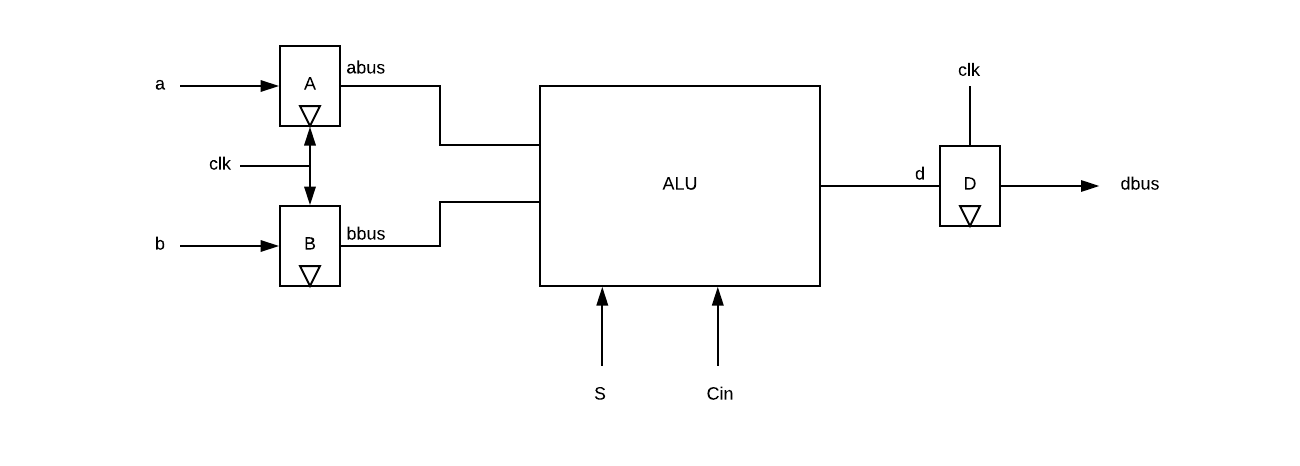
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EECE 3324

Lab 2

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1. Description
   1. The main purpose of this lab was to extend the basic ALU design created in lab 1 by adding “pipelined” inputs and outputs. The pipeline synchronizes the whole input and output structure to a single clock cycle. This means that in future assignments, we will be able to execute multiple instructions at once when more modules are added to the entire structure.
2. Block Diagram
   1. Below shows the block diagram of the pipelined ALU.



1. Steps needed to complete the Lab
   1. The main difference between a normal ALU and the pipelined ALU created in Lab 2 is the synchronization on input and output to a single clock cycle. The specification was to provide an output in less than 20 ns of time with a 40 MHz clock frequency. This meant that the clock cycle was 25 ns with a half cycle of 12.5 ns. On the positive edge of each clock cycle (every 12.5 seconds), the value stored in the pipeline would be pushed into the corresponding output. This specification required the creation of a D Flip-Flop, whose output takes the value of the input on a specified clock edge, either the rising or falling edge. This module was constructed and added to the original ALU structure. The order of which the modules were instantiated was such that that inputs were instantiated first, and then the output D Flip-Flop module was instantiated after the ALU module was instantiated. This was done so that the ALU populated the value of the output before the value was pushed into the bus.
2. Lessons Learned
   1. Throughout this lab, I learned the importance of having a pipelined ALU, and how this structure is an essential building block of some processors. Also, examining how the order of module instantiation affects output in Verilog is something that will need to be taken into consideration during future labs.